P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-20V	±12V	20mR@-4V5	-7A
		25mR@-2V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits.

➢ Applications

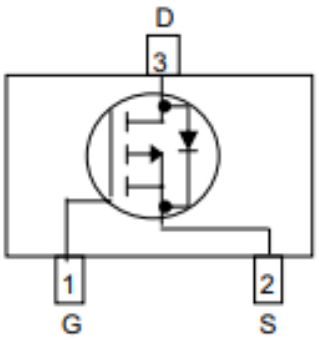
- Load Switch
- Portable Devices
- DCDC conversion

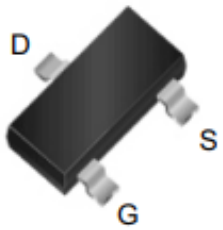
➢ Ordering Information

Device	Package	Shipping
SSC8123GS6A	SOT23-3L	3000/Reel

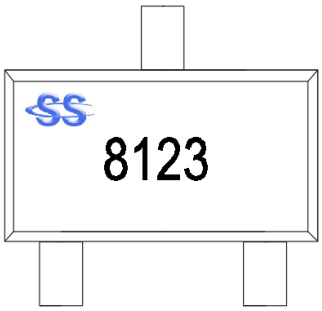
➢ Pin configuration

Top view





SOT23-3L



Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	±12	V
I_D	Continuous Drain Current [a]	-7	A
I_{DM}	Pulsed Drain Current [b]	-21	A
P_D	Power Dissipation [c]	1.6	W
T_J	Operation junction temperature	-55 to 150	℃
T_{STG}	Storage temperature range	-55 to 150	℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	78	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design.

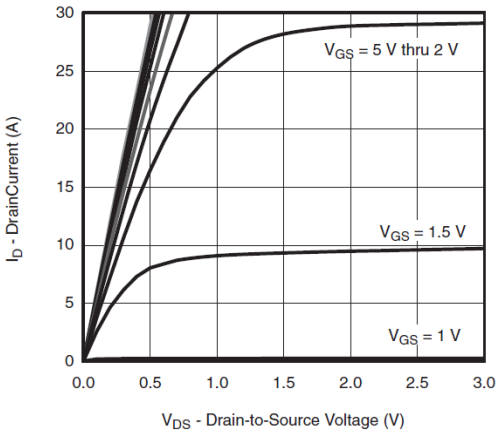
b. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using steady state junction-to-ambient thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

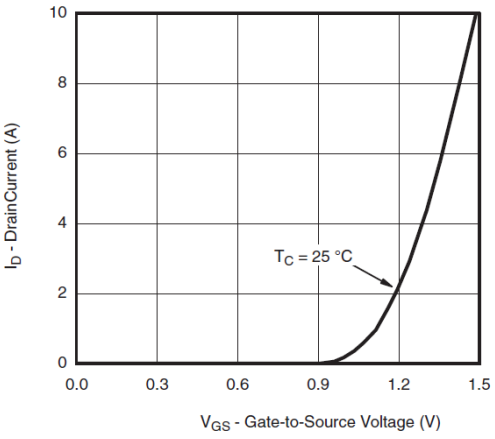
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V, ID=-250uA	-20			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS, ID=-250uA	-0.4	-0.7	-0.9	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-4.5V, ID=-5A		20	26	mR
		VGS=-2.5V, ID=-3A		25	36	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-16V, VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±12V, VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V, ID=-5A		10		S
V_{SD}	Forward Voltage	VGS=0V, IS=-2A		-0.78	-1.2	V
Ciss	Input Capacitance	VDS=-10V, VGS=0V, f=1MHz		1430		pF
Coss	Output Capacitance			182		
Crss	Reverse Capacitance			160		
$T_{D(ON)}$	Turn-on delay time	VDS=-10V, VGEN=-4.5V, RL=1.43R RG=3R		11		ns
Tr	Rise Time			18		
$T_{D(OFF)}$	Turn-off delay time			45		
Tf	Fall Time			23		
Qg	Total Gate charge	VGS=-4.5V, VDS=-10V ID=-7A		15		nC
Qgs	Gate Source charge			3		
Qgd	Gate Drain charge			4		

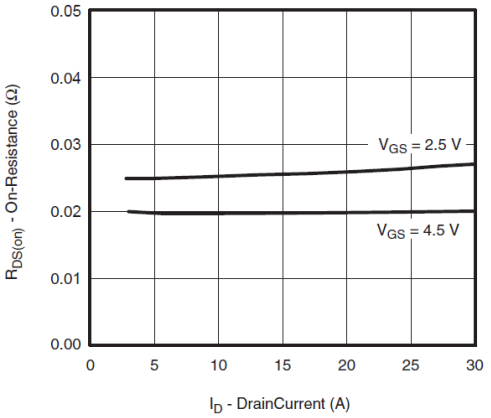
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)



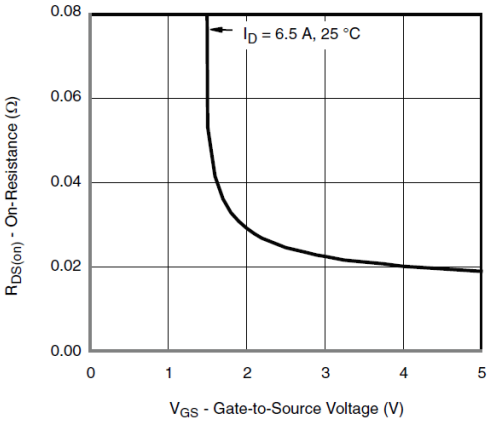
Output Characteristics



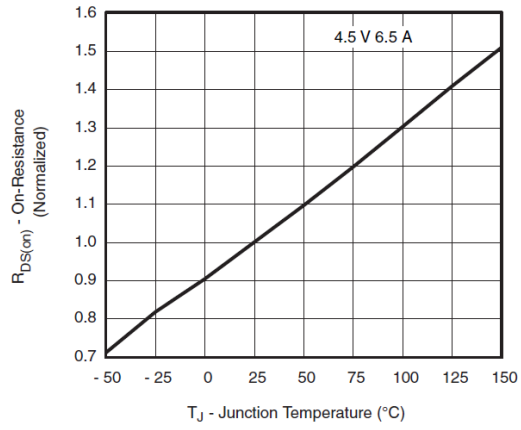
Transfer Characteristics



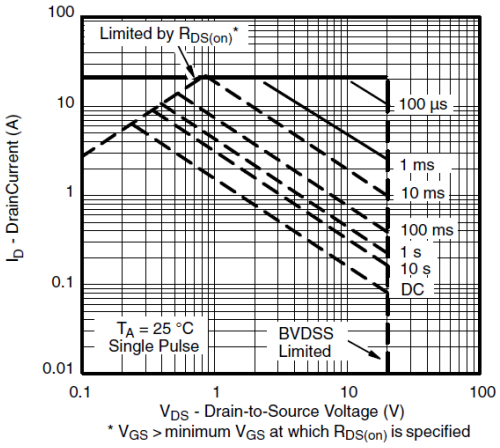
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

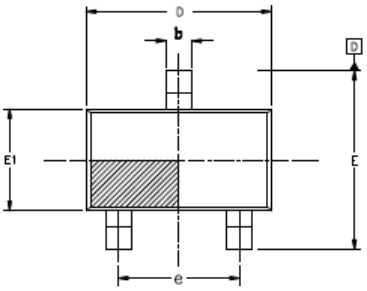


On-Resistance vs. Junction Temperature

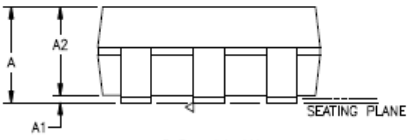


Safe Operating Area, Junction-to-Ambient

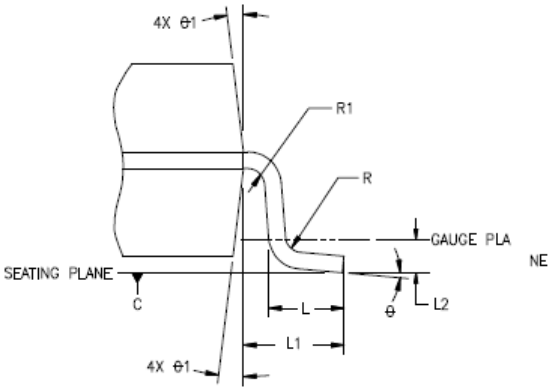
➢ Package Information

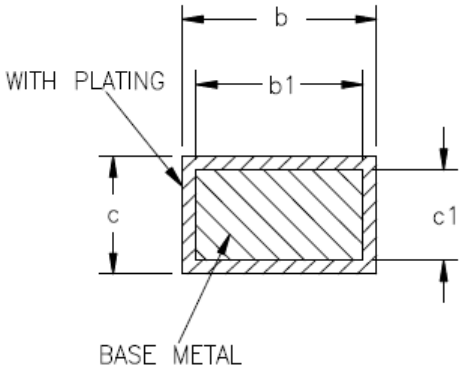


TOP VIEW



SIDE VIEW





SYMBOL	MIN	NOM	MAX
A	--	--	1.35
A1	0	--	0.15
A2	1.0	1.1	1.2
b	0.35	--	0.45
b1	0.32	--	0.38
c	0.14	--	0.20
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	1.8	1.9	2.0
L	0.35	0.45	0.6
L1	0.6REF		
L2	0.25REF		
R	0.1	--	--
R1	0.1	--	--
θ	0°	4°	8°
θ1	5°	10°	15°

NOTES:
1.All DIMENSIONS REFER TO JEDEC STANDARD MO-178
2.DIMENSION D DOES NOT INCLUDE MOLD FLASH
3.DIMENSION E1 DOSE NOT INCLUDE MOLD FLASH
4.FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.

SOT23-3L

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